**IN THE CLAIMS:**

Please cancel claims 1-20 without prejudice or disclaimer as to the subject matter contained therein.

Please add new claims 21-41as shown in the following claims listing.

Claims 1-20. (Cancelled)

21. (New) A semiconductor device for use in a computing system, the semiconductor device comprising:

a plurality of processors formed on the semiconductor device;

a plurality of input/output (I/O) controllers formed on the semiconductor device and coupled to the plurality of processors such that each of the plurality of processors is coupled to each of the plurality of I/O controllers; and

a plurality of I/O interfaces formed on the semiconductor device and coupled to convey the data between the plurality of I/O controllers and the computing system;

wherein the plurality of I/O controllers are arranged to form a switching fabric including a plurality of communication channels configured to convey data between any of the processors and any of the (I/O) interfaces;

wherein at least a portion of the processors and at least a portion of the I/O controllers are redundant.

22. (New) The semiconductor device of claim 21, further comprising a controller configured to detect a failure of any of the plurality of processors and any of the plurality of I/O controllers.

23. (New) The semiconductor device of claim 22, wherein the controller is further configured to remove from service a given processor in response to detecting a failure in the given processor.

24. (New) The semiconductor device of claim 22, wherein in response to detecting a failure of a given processor, the controller is further configured to cause a given redundant processor to perform operations associated with a failed processor.

25. (New) The semiconductor device of claim 22, wherein the controller is further configured to cause one or more of the redundant processors to be disabled and placed in a wait state.

26. (New) The semiconductor device of claim 22, wherein the controller is further configured to cause one or more of the redundant processors to be enabled and placed in a wait state.

27. (New) The semiconductor device of claim 22, wherein the controller is further configured to cause one or more of the redundant processors to be disabled by disabling a clock signal used to clock the one or more of the redundant processors.

28. (New) The semiconductor device of claim 22, wherein the controller is further configured to cause one or more of the redundant processors to run real-time diagnostics for the computing system.

29. (New) The semiconductor device of claim 22, wherein the controller is further configured to cause one or more of the redundant processors to manage failover functions of the processor-based system.

30. (New) The semiconductor device of claim 21, further comprising a crossbar configured to interconnect each of the plurality of processors to each of the plurality of I/O controllers.

31. (New) The semiconductor device of claim 21, wherein the switching fabric is configured to interconnect each I/O controller of the plurality of I/O controllers to at least two I/O interfaces of the plurality of I/O interfaces.

32. (New) The semiconductor device of claim 21, wherein the switching fabric is configured to interconnect each I/O controller to each I/O interface of the plurality of I/O interfaces.

33. (New) A method comprising:

forming a plurality of processors on the semiconductor device;

forming a plurality of input/output (I/O) controllers on the semiconductor device;

interconnecting each of the plurality of processors to each of the plurality of I/O controllers; and

forming a plurality of I/O interfaces on the semiconductor device for interconnecting the plurality of I/O controllers and the computing system;

forming a switching fabric by arranging the plurality of I/O controllers and including a plurality of communication channels configured to convey data between any of the processors and any of the (I/O) interfaces;

wherein at least a portion of the processors and at least a portion of the I/O controllers are redundant.

34. (New) The method of claim 33, further comprising detecting a failure of any of the plurality of processors and any of the plurality of I/O controllers.

35. (New) The method of claim 34, removing from service a given processor in response to detecting a failure in the given processor.

36. (New) The method of claim 33, wherein in response to detecting a failure of a given processor, causing a given redundant processor to perform operations associated with the failed processor.

37. (New) The method of claim 33, further comprising causing one or more of the redundant processors to be disabled and placed in a wait state.

38. (New) The method of claim 33, further comprising causing one or more of the redundant processors to be enabled and placed in a wait state.

39. (New) The method of claim 33, further comprising causing one or more of the redundant processors to be disabled by disabling a clock signal used to clock the one or more of the redundant processors.

40. (New) The method of claim 22, further comprising causing one or more of the redundant processors to run real-time diagnostics for the computing system.

41. (New) The method of claim 22, further comprising causing one or more of the redundant processors to manage failover functions of the processor-based system.